IN THE CLAIMS

1. (Original) A multiphase clock generator comprising:

a first clock divider for generating a first-phase clock signal from a first input clock signal;

a first logic gate connected to an output port of the first clock divider;

a second clock divider connected to an output port of the first logic gate, the second clock divider for generating a second-phase clock signal from the first input clock signal;

a second logic gate connected to an output port of the second clock divider; and

a third clock divider connected to an output port of the second logic gate, the third clock divider for generating a third-phase clock signal from a second input clock signal.

2. (Currently amended) The clock generator of claim 1, wherein the first clock generator and second clock generators each divide a frequency of the first input clock signal by two, and the third clock generator divides a frequency of the second input clock signal by two.

3. (Original) The clock generator of claim 1, further comprising:

a first inverter connected between an input port of the first clock divider and the first input clock signal;

a second inverter connected between an output port of the first logic gate and an input port of the second clock divider; and

a third inverter connected between an output port of the second logic gate and an input port of the third clock divider.

4. (Original) The clock generator of claim 1, wherein a first input port of the second logic gate is for receiving a reset signal, a second input port of the second logic gate is connected to the output port of the second clock divider for receiving the second-phase clock signal therefrom, and a third input port of the second logic gate is for receiving the second input clock signal.

5. (Original) The clock generator of claim 4, further comprising a repeater connected between the third input port of the second logic gate and the second input clock signal.

6. (Original) The clock generator of claim 4, wherein:

a logic value of an output of the second logic gate is low when logic values of the reset signal at the first input port and the second-phase clock signal at the second input port are both low, regardless of whether a logic value of the second input clock signal at the third input port is high or low;

the logic value of the output of the second logic gate is high when the logic values of the second-phase clock signal at the second input port and the second input clock signal at the third input port are both high, regardless of whether the logic value of the reset signal at the first input port is low or high; and

the logic value of the output of the second logic gate stays at the logic value of output of the second logic gate from when the logic values of the reset signal at the first input port and the second-phase clock signal at the second input port were last low or from when the logic values of the second-phase clock signal at the second input port and the second input clock signal at the third input port were last high for all other combinations of the logic values of the reset signal, the second-phase clock signal, and the second input clock signal respectively at the first, second, and third input ports.

7. (Original) The clock generator of claim 1, wherein the first logic gate comprises first and second input ports, the first input port is connected to the output port of the first clock divider for receiving the first-phase clock signal therefrom, and the second input port is for receiving a reset signal.

8. (Original) The clock generator of claim 7, wherein:

a logic value of an output of the first logic gate is low when logic values of the first-phase clock signal at the first input port and the reset signal at the second input port are both low;

the logic value of the output of the first logic gate is high when the logic values of the first-phase clock signal at the first input port and the reset signal at the second input port are both high; and

when the logic value of the first-phase clock signal at the first input port and the reset signal at the second input port are different from each other, the logic value of the output of the first logic gate stays at the logic value of the output of the first logic gate from when the first-phase clock signal at the first input port and the reset signal at the second input port were last low or were last high.

9. (Original) The clock generator of claim 1, further comprising:

a third logic gate connected to an output port of the third clock divider; and

a fourth clock divider connected to an output port of the third logic gate, the fourth clock divider for generating a fourth-phase clock signal from the second input clock signal.

10. (Original) The clock generator of claim 9, further comprising an inverter connected between an output port of the third logic gate and an input port of the fourth clock divider.

11. (Original) A multiphase clock generator comprising:

a first clock divider for generating a first-phase clock signal from a first input clock signal, an input port of the first clock divider connected to a first inverter for receiving the first input clock signal;

a first logic gate connected to an output port of the first clock divider;

a second clock divider connected to an output port of the first logic gate through a second inverter, the second clock divider for generating a second-phase clock signal from the first input clock signal;

a second logic gate connected to an output port of the second clock divider;

a third clock divider connected to an output port of the second logic gate through a third inverter, the third clock divider for generating a third-phase clock signal from a second input clock signal;

a third logic gate connected to an output port of the third clock divider; and

a fourth clock divider connected to an output port of the third logic gate through a fourth inverter, the fourth clock divider for generating a fourth-phase clock signal from the second input clock signal.

12. (Original) The clock generator of claim 11, wherein the first and second clock generators divide a frequency of the first input clock signal by two, and the third and fourth clock generators divide a frequency of the second input clock signal by two.

13. (Original) The clock generator of claim 11, further comprising a repeater connected between an input port of the second logic gate the second input clock signal.

14. (Original) The clock generator of claim 11, wherein:

the first logic gate comprises first and second input ports, the first input port is connected to the output port of the first clock divider for receiving the first-phase clock signal therefrom, and the second input port is for receiving a reset signal;

the second logic gate comprises third, fourth, and fifth input ports, the third input port is for receiving the reset signal, the fourth input port is connected to the output port of the second clock divider for receiving the second-phase clock signal therefrom, and the fifth input port is for receiving the second input clock signal; and

the third logic gate comprises sixth and seventh input ports, the sixth input port is connected to the output port of the third clock divider for receiving the third-phase clock signal therefrom, and the seventh input port is for receiving the reset signal.

15. (Original) The clock generator of claim 11, wherein:

when the first or third logic gate receives two inputs having a common logic value, an output of the first or third logic gate is the common logic value; and

when the first or third logic gate receives two inputs having different logic values, the output of the first or third logic gate is the common logic value from the last time the first or third logic gate received two inputs having the common logic value.

16. (Original) The clock generator of claim 11, wherein:

an output of the second logic gate is a logic low value when first and second inputs of the second logic gate are logic low values, regardless of whether a third input of the second logic gate is a logic low or high value;

wherein the output of the second logic gate is a logic high value when the second and third inputs of the second logic gate are logic high values, regardless of whether the first input of the second logic gate is a logic low or high value; and

wherein the output of the second logic gate stays at the logic value from when the first and second inputs of the second logic gate were last at logic low values or from when the second and third inputs of the second logic gate were last at logic high values for all other combinations of the logic values of the first, second, and third inputs of the second logic gate.

17. (Original) A memory device comprising:

an array of memory cells; and

control circuitry for controlling access to the array of memory cells, the control circuitry comprising a multiphase clock generator, the multiphase clock generator comprising:

a first clock divider for generating a first-phase clock signal from a first input clock signal;

a first logic gate connected to an output port of the first clock divider;

a second clock divider connected to an output port of the first logic gate, the second clock divider for generating a second-phase clock signal from the first input clock signal;

a second logic gate connected to an output port of the second clock divider; and

a third clock divider connected to an output port of the second logic gate, the third clock divider for generating a third-phase clock signal from a second input clock signal.

18. (Original) The memory device of claim 17, wherein:

the first logic gate comprises first and second input ports, the first input port is connected to the output port of the first clock divider for receiving the first-phase clock signal therefrom, and the second input port is for receiving a reset signal; and

the second logic gate comprises third, fourth, and fifth input ports, the third input port is for receiving the reset signal, the fourth input port is connected to the output port of the second clock divider for receiving the second-phase clock signal therefrom, and the fifth input port is for receiving the second input clock signal.

19. (Original) The memory device of claim 17, wherein:

when the first logic gate receives two inputs having a common logic value, an output of the first logic gate is the common logic value; and

when the first logic gate receives two inputs having different logic values, the output of the first logic gate is the common logic value from the last time the first logic gate received two inputs having the common logic value.

20. (Original) The memory device of claim 17, wherein:

an output of the second logic gate is a logic low value when first and second inputs of the second logic gate are logic low values, regardless of whether a third input of the second logic gate is a logic low or high value;

the output of the second logic gate is a logic high value when the second and third inputs of the second logic gate are logic high values, regardless of whether the first input of the second logic gate is a logic low or high value; and

the output of the second logic gate stays at the logic value from when the first and second inputs of the second logic gate were last at logic low values or from when the second and third inputs of the second logic gate were last at logic high values for all other combinations of the logic values of the first, second, and third inputs of the second logic gate.

21. (Original) A memory device comprising:

an array of memory cells; and

control circuitry for controlling access to the array of memory cells, the control circuitry comprising a multiphase clock generator, the multiphase clock generator comprising:

a first clock divider for generating a first-phase clock signal from a first input clock signal, an input port of the first clock divider connected to a first inverter for receiving the first input clock signal;

a first logic gate connected to an output port of the first clock divider;

a second clock divider connected to an output port of the first logic gate through a second inverter, the second clock divider for generating a second-phase clock signal from the first input clock signal;

a second logic gate connected to an output port of the second clock divider;

a third clock divider connected to an output port of the second logic gate through a third inverter, the third clock divider for generating a third-phase clock signal from a second input clock signal;

a third logic gate connected to an output port of the third clock divider; and

a fourth clock divider connected to an output port of the third logic gate through a fourth inverter, the fourth clock divider for generating a fourth-phase clock signal from the second input clock signal.

22. (Original) The memory device of claim 21, wherein:

the first logic gate comprises first and second input ports, the first input port is connected to the output port of the first clock divider for receiving the first-phase clock signal therefrom, and the second input port is for receiving a reset signal;

the second logic gate comprises third, fourth, and fifth input ports, the third input port is for receiving the reset signal, the fourth input port is connected to the output port of the second clock divider for receiving the second-phase clock signal therefrom, and the fifth input port is for receiving the second input clock signal; and

the third logic gate comprises sixth and seventh input ports, the sixth input port is connected to the output port of the third clock divider for receiving the third-phase clock signal therefrom, and the seventh input port is for receiving the reset signal.

23. (Original) The memory device of claim 21, wherein:

when the first or third logic gate receives two inputs having a common logic value, an output of the first or third logic gate is the common logic value; and

when the first or third logic gate receives two inputs having different logic values, the output of the first or third logic gate is the common logic value from the last time the first or third logic gate received two inputs having the common logic value.

24. (Original) The memory device of claim 21, wherein:

an output of the second logic gate is a logic low value when first and second inputs of the second logic gate are logic low values, regardless of whether a third input of the second logic gate is a logic low or high value;

the output of the second logic gate is a logic high value when the second and third inputs of the second logic gate are logic high values, regardless of whether the first input of the second logic gate is a logic low or high value; and

the output of the second logic gate stays at the logic value from when the first and second inputs of the second logic gate were last at logic low values or from when the second and third inputs of the second logic gate were last at logic high values for all other combinations of the logic values of the first, second, and third inputs of the second logic gate.

25. (Original) A memory system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

an array of memory cells; and

control circuitry for controlling access to the array of memory cells, the control circuitry comprising a multiphase clock generator, the multiphase clock generator comprising:

a first clock divider for generating a first-phase clock signal from a first input clock signal;

a first logic gate connected to an output port of the first clock divider;

a second clock divider connected to an output port of the first logic gate, the second clock divider for generating a second-phase clock signal from the first input clock signal;

a second logic gate connected to an output port of the second clock divider; and

a third clock divider connected to an output port of the second logic gate, the third clock divider for generating a third-phase clock signal from a second input clock signal.

26. (Original) The memory system of claim 25, wherein a first input port of the second logic gate is for receiving a reset signal, a second input port of the second logic gate is connected to the output port of the second clock divider for receiving the second-phase clock signal therefrom, and a third input port of the second logic gate is for receiving the second input clock signal.

27. (Original) The memory system of claim 26, wherein:

a logic value of an output of the second logic gate is low when logic values of the reset signal at the first input port and the second-phase clock signal at the second input

port are both low, regardless of whether a logic value of the second input clock signal at the third input port is high or low;

the logic value of the output of the second logic gate is high when the logic values of the second-phase clock signal at the second input port and the second input clock signal at the third input port are both high, regardless of whether the logic value of the reset signal at the first input port is low or high; and

the logic value of the output of the second logic gate stays at the logic value of output of the second logic gate from when the logic values of the reset signal at the first input port and the second-phase clock signal at the second input port were last low or from when the logic values of the second-phase clock signal at the second input port and the second input clock signal at the third input port were last high for all other combinations of the logic values of the reset signal, the second-phase clock signal, and the second input clock signal respectively at the first, second, and third input ports.

28. (Original) The memory system of claim 25, wherein the first logic gate comprises first and second input ports, the first input port is connected to the output port of the first clock divider for receiving the first-phase clock signal therefrom, and the second input port is for receiving a reset signal.

29. (Original) The memory system of claim 28, wherein:

a logic value of an output of the first logic gate is low when logic values of the first-phase clock signal at the first input port and the reset signal at the second input port are both low;

the logic value of the output of the first logic gate is high when the logic values of the first-phase clock signal at the first input port and the reset signal at the second input port are both high; and

when the logic value of the first-phase clock signal at the first input port and the reset signal at the second input port are different from each other, the logic value of the output of the first logic gate stays at the logic value of the output of the first logic gate from when the first-phase clock signal at the first input port and the reset signal at the second input port were last low or were last high.

30. (Original) A memory system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

an array of memory cells; and

control circuitry for controlling access to the array of memory cells, the control circuitry comprising a multiphase clock generator, the multiphase clock generator comprising:

a first clock divider for generating a first-phase clock signal from a first input clock signal, an input port of the first clock divider connected to a first inverter for receiving the first input clock signal;

a first logic gate connected to an output port of the first clock divider;

a second clock divider connected to an output port of the first logic gate through a second inverter, the second clock divider for generating a second-phase clock signal from the first input clock signal;

a second logic gate connected to an output port of the second clock divider;

a third clock divider connected to an output port of the second logic gate through a third inverter, the third clock divider for generating a third-phase clock signal from a second input clock signal;

a third logic gate connected to an output port of the third clock divider; and

a fourth clock divider connected to an output port of the third logic gate through a fourth inverter, the fourth clock divider for generating a fourth-phase clock signal from the second input clock signal.

31. (Original) The memory system of claim 30, wherein:

the first logic gate comprises first and second input ports, the first input port is connected to the output port of the first clock divider for receiving the first-phase clock signal therefrom, and the second input port is for receiving a reset signal;

the second logic gate comprises third, fourth, and fifth input ports, the third input port is for receiving the reset signal, the fourth input port is connected to the output port of the second clock divider for receiving the second-phase clock signal therefrom, and the fifth input port is for receiving the second input clock signal; and

the third logic gate comprises sixth and seventh input ports, the sixth input port is connected to the output port of the third clock divider for receiving the third-phase clock signal therefrom, and the seventh input port is for receiving the reset signal.

32. (Original) The memory system of claim 30, wherein:

when the first or third logic gate receives two inputs having a common logic value, an output of the first or third logic gate is the common logic value; and

when the first or third logic gate receives two inputs having different logic values, the output of the first or third logic gate is the common logic value from the last time the first or third logic gate received two inputs having the common logic value.

33. (Original) The memory system of claim 30, wherein:

an output of the second logic gate is a logic low value when first and second inputs of the second logic gate are logic low values, regardless of whether a third input of the second logic gate is a logic low or high value;

the output of the second logic gate is a logic high value when the second and third inputs of the second logic gate are logic high values, regardless of whether the first input of the second logic gate is a logic low or high value; and

the output of the second logic gate stays at the logic value from when the first and second inputs of the second logic gate were last at logic low values or from when the second and third inputs of the second logic gate were last at logic high values for all other combinations of the logic values of the first, second, and third inputs of the second logic gate.

34. (Original) A method of operating a multiphase clock generator, the method comprising:

starting a first-phase clock signal at a first clock edge of a first input clock signal;

at least one clock cycle of the first input clock signal after starting the first-phase clock signal, starting a second-phase clock signal at a second clock edge of the first input clock signal;

after starting the second-phase clock signal, starting a third-phase clock signal at a first clock edge of a second input clock signal so that a clock edge of the third-phase clock signal occurs a half a clock cycle of the first input clock signal after a clock edge of the first-phase clock signal and the half the clock cycle of the first input clock signal before a clock edge of the second-phase clock signal, wherein the first and second input clock signals have the same frequency and are half the clock cycle of the first input clock signal out of phase, wherein the clock edges of the first- second-, and third-phase clock signals are like clock edges; and

at least one clock cycle of the first input clock signal after starting the third-phase clock signal, starting a fourth-phase clock signal at a second clock edge of the second input clock signal so that a clock edge of the fourth-phase clock signal occurs the

half the clock cycle of the first input clock signal after the clock edge of the second-phase clock signal, wherein the clock edges of the second- and fourth-phase clock signals are like clock edges.

35. (Original) The method of claim 34, further comprising removing a first clock divider from a reset state before starting the first-phase clock signal.

36. (Original) The method of claim 34, further comprising removing a second clock divider from a reset state before starting the second-phase clock signal.

37. (Original) The method of claim 34, further comprising removing a third clock divider from a reset state before starting the third-phase clock signal.

38. (Original) The method of claim 34, further comprising removing a fourth clock divider from a reset state before starting the fourth-phase clock signal.

39. (Original) A method of operating a multiphase clock generator, the method comprising:

inverting a first logic-high reset signal at a first inverter of the clock generator to produce a first logic-low reset signal;

receiving the first logic-low reset signal at a first clock divider of the clock generator from the first inverter;

after receiving the first logic-low reset signal at the first clock divider, starting a first-phase clock signal at the first clock divider at a first clock edge of a first input clock signal received at the first clock divider;

receiving the first logic-high reset signal at a first logic gate of the clock generator;

receiving the first-phase clock signal at the first logic gate from the first clock divider;

sending a second logic-high reset signal from the first logic gate to a second inverter of the clock generator when the first-phase clock signal is a logic high;

inverting the second logic-high reset signal at the second inverter to produce a second logic-low reset signal;

receiving the second logic-low reset signal at a second clock divider of the clock generator from the second inverter;

after receiving the second logic-low reset signal at the second clock divider and at least one clock cycle of the first input clock signal after starting the first-phase clock signal, starting a second-phase clock signal at the second clock divider at a second clock edge of the first input clock signal received at the second clock divider;

receiving the first logic-high reset signal at a second logic gate of the clock generator;

receiving the second-phase clock signal at the second logic gate from the second clock divider;

receiving a second input clock signal at the second logic gate;

sending a third logic-high reset signal from the second logic gate to a third inverter of the clock generator when the second-phase clock signal and the second input clock signal are both logic highs;

inverting the third logic-high reset signal at the third inverter to produce a third logic-low reset signal;

receiving the third logic-low reset signal at a third clock divider of the clock generator from the third inverter;

after receiving the third logic-low reset signal at the third clock divider and after starting the second-phase clock signal, starting a third-phase clock signal at the third clock divider at a first clock edge of the second input clock signal received at the third clock divider so that a clock edge of the third-phase clock signal occurs a half a clock cycle of the first input clock signal after a clock edge of the first-phase clock signal and the half the clock cycle of the first input clock signal before a clock edge of the second-phase clock signal, wherein the first and second input

clock signals have the same frequency and are half the clock cycle of the first input clock signal out of phase, wherein the clock edges of the first-, second-, and third-phase clock signals are like clock edges;

receiving the first logic-high reset signal at a third logic gate of the clock generator;

receiving the third-phase clock signal at the third logic gate from the third clock divider;

sending a fourth logic-high reset signal from the third logic gate to a fourth inverter of the clock generator when the third-phase clock signal is a logic high;

inverting the fourth logic-high reset signal at the fourth inverter to produce a fourth logic-low reset signal;

receiving the fourth logic-low reset signal at a fourth clock divider of the clock generator from the fourth inverter; and

after receiving the fourth logic-low reset signal at the fourth clock divider and at least one clock cycle of the first input clock signal after starting the third-phase clock signal, starting a fourth-phase clock signal at the fourth clock divider at a second clock edge of the second input clock signal received at the fourth clock divider so that a clock edge of the fourth-phase clock signal occurs the half the clock cycle of the first input clock signal after the clock edge of the second-phase clock signal, wherein the clock edges of the second- and fourth-phase clock signals are like clock edges.